Remarks

This amendment is in response to the Office Action dated October 24, 2002. Claims 1 and 2 have been amended, claim 11 canceled without prejudice, and new claims 12-21 have been added. Claims 1-10 and 12-21 are currently pending. Reexamination and reconsideration are respectfully requested.

Claim 11 was canceled without prejudice as being a non-elected claim.

Claims 1-10 were rejected under 35 U.S.C. 102(b) or 103(a) as unpatentable over U.S. Patent No. 5,789,791 to Bergemont (hereinafter "Bergemont"). The rejection is respectfully traversed. Applicant does not agree with the Examiner's characterization of Bergemont including, for example, the Examiner's statements regarding the teachings and suggestions of Bergemont and the number of connection sections, which will be discussed below.

Regarding claim 1, applicant respectfully submits that the Examiner cited no portion of Bergemont that describes or suggests a structure including "an element region at least partially surrounded by an element isolation region" and "at least two connection sections that connect the signal line to the gate electrode layer, wherein at least one connection section is positioned outside of the element region and at least one connection is positioned in the element region" as recited in claim 1. Applicant notes that from Bergemont Fig 4, for example, it appears that there are no connections to the gate 122 other than those at the end regions through the vias 134 and including the first metal regions 132 and gate contact 130. Accordingly, applicant respectfully requests that the rejection of claim 1 be withdrawn.

Claim 2 and its dependent claims 3-8 can be distinguished at least in a similar manner as claim 1.

Regarding claim 9, applicant respectfully submits that the Examiner cited no portion of the art that describes or suggests a structure "wherein at least two of the plurality of transistors have a different number of connection sections" as recited in claim 9. Applicant notes that as described in the specification at, for example, pages 20-25, certain embodiments include "a different number of connection sections." By having a different number of connection sections, for example, the transistors have a different timing for starting switching operations, which can lead to one or more benefits as described in the specification. The Examiner cited no portion of

Bergemont that describes or suggests such an issue as recited in the claims. Accordingly, for at least the reasons in this paragraph, applicant respectfully requests that the rejection of claim 9 and its dependent claim 10 be withdrawn.

New claims 12-21 have been added. Support for these claims may be found throughout the specification and original claims. It is believed that no new matter has been entered. Examination is respectfully requested.

Attached hereto is a marked-up version of the claim changes made by the present amendment. The attached page is captioned "Version with markings to show changes made."

Applicant respectfully submits that for at least the above reasons claims 1-10 and 12-21 are in patentable form. Reexamination and reconsideration are respectfully requested. If, for any reason, the application is not in condition for allowance, the Examiner is requested to telephone the undersigned to discuss the steps necessary to place the application into condition for allowance.

Respectfully submitted,

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Alan S. Raynes — March 24, 2003

Alan S. Raynes **(Date)**

Version With Markings to Show Changes Made

Claims 1-2 were amended as follows:

1. (amended) A driver circuit comprising a semiconductor integrated circuit having a transistor in which a drive signal is applied to the transistor to drive the transistor to thereby drive a load, the driver circuit comprising:

an element region at least partially surrounded by an element isolation region;

a signal line that supplies the drive signal to the transistor, the signal line extending across the element region; [being separated from the transistor by a dielectric layer; and]

a dielectric layer formed in the element region;

a gate electrode layer, wherein part of the gate electrode layer is positioned on the dielectric layer in the element region and part of the gate electrode layer is positioned outside of the element region; and

at least two connection sections that connect the signal line to [a] the gate electrode layer [of the transistor], wherein at least one connection section is positioned outside of the element region and at least one connection section is positioned in the element region [the connection sections being provided in a width direction of the gate electrode].

2. (amended) A driver circuit comprising a semiconductor integrated circuit having a plurality of transistors in which a single drive signal is applied to each of the transistors to drive the transistors to thereby drive a load, the driver circuit comprising:

an element region at least partially surrounded by an element isolation region;

a signal line for each of the transistors that supplies the drive signal and extends across the element region; [, the signal lines being separated from each of the transistors by a dielectric layer,]

a dielectric layer in the element region for each of the transistors;

a gate electrode layer on the dielectric layer in the element region for each of the transistors, wherein part of the gate electrode layer extends to outside of the element region; and

at least two connection sections that connect the signal line to the gate electrode [of] for at least one of the transistors, wherein a first of the at least two connection sections is positioned

outside of the element region and a second of the at least two connections sections is positioned in the element region [the connection sections being provided in a width direction of the gate electrode].